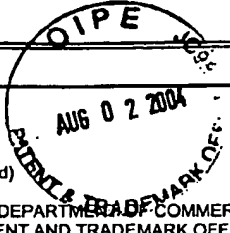


Sheet 1 of 1							
<div style="text-align: center;">  </div> <p>FORM PTO 1449 (modified)</p> <p>U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE</p> <p>LIST OF REFERENCES CITED BY APPLICANT(S) (Use several sheets if necessary)</p>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">ATTY DOCKET NO. <b>BHT/3230-63</b></td> <td style="width: 50%;">APPLICATION NO. <b>10/625,516</b></td> </tr> <tr> <td colspan="2">APPLICANT <b>TSUI</b></td> </tr> <tr> <td>FILING DATE <b>July 24, 2003</b></td> <td>GROUP <b>2813</b></td> </tr> </table>	ATTY DOCKET NO. <b>BHT/3230-63</b>	APPLICATION NO. <b>10/625,516</b>	APPLICANT <b>TSUI</b>		FILING DATE <b>July 24, 2003</b>	GROUP <b>2813</b>
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CAT		C.J. Koeneke, et al.; "Schottky MOSFET for VLSI"; in Dig. of IEDM, p. 367; 1981					
CAT		S.E. Swirhun et al.; "A VLSI Suitable Schottky Barrier CMOS Process"; IEEE, Trans. Electron Devices; Vol. ED-32, No. 2; p. 194; 1985					
CAT		B.Y. Tsui et al.; "A Novel Process For High-Performance Schottky Barrier PMOS"; J. Electrochem. Soc.; Vol. 136, No. 5; p. 1456; 1989					
CAT		C. Wang et al.; "Sub-50-nm PtSi Schottky Source/Drain p-MOSFETs"; in Proc. of Device Research Conf.; p.72; 1998					
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CAT		W. Saitoh et al. ; "35 nm Metal Gate SOI-p-MOSFETs With PtSi Schottky Source/Drain"; In Proc. of Device Research Conf.; p. 30; 1999					
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EXAMINER <i>Craig A. Thompson</i>		DATE CONSIDERED <i>8/20/04</i>					

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Sheet 1 of 1

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APPLICANT TSUI

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